USN					

M.Tech. Degree Examination, June/July 2013 **Advances in VLSI Design**

- I im	ie: (3 hrs. Max. N	1arks: 100
	1	Note: Answer any FIVE full questions.	-(0)
1	a	What are MOS devices? Explain saturation, linear and cut-off regions using d	rain current
•	٠.,	equations for MOS devices.	(10 Marks)
	b.	Compare CMOS and BiCMOS technologies.	(06 Marks)
	c.	Discuss CMOS device aspect ratio.	(04 Marks)
	٥.	Discuss whos device aspect tario.	(04 Maiks)
2	a.	With neat diagram, explain how MESFET reaches pinch-off and saturation.	(10 Marks)
~	b.	Derive a drain current (ID) of JFET extended to MESFET using its quantitative	• •
	υ.	Of STET extended to WESTET daying its quantitative	(10 Marks)
			(55 11.11.1.)
3	a.	Explain MIS system in equilibrium.	(06 Marks)
	b.	Calculate the threshold voltage for realistic n-channel MIS system device	
		following: $N_a = 10^{17} \text{cm}^{-3}$, $Q_i = 10^{11} \text{ q/cm}^2$, $d = 20 \text{nm}$, $\psi_{ms} = -0.95 \text{ V}$.	(08 Marks)
	c.	Explain small signal model operation of MOSFET.	(06 Marks)
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4	a.	Using mobility, transit time and drain current explain short channel effect.	(12 Marks)
	b.	What is proximity effect? Explain processing challenges for CMOS miniaturization	
	••		(08 Marks)
5	a.	Explain carbon nanotubes.	(08 Marks)
	b.	Discuss molecular diode under forward bias and reverse bias.	(08 Marks)
	c.	Write note on direct tolerant computing.	(04 Marks)
6	a.	With the help of long polysilicon line, derive an expression for propagation delay	. (10 Marks)
	b.	Explain designing of pass transistor logic for NMOS, PMOS and CMOS.	(10 Marks)
7	a.	Realize 4-bit tree network using tally circuit and write its stick diagram.	(10 Marks)
	b.	Realize the static AOI gates in NMOS and CMOS technology for the following:	
		Y = (AB + CD).	(06 Marks)
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(04 Marks) c Explain chip architecture.

- Explain the following:
 - Regularity and modularity.
 - b. Programmable structure.
 - CMOS design method.
 - d. Full custom design. (20 Marks)